AMENDMENTS TO THE CLAIMS

Claims 1-58. (Cancelled)

59. (Previously Presented) An integrated circuit substrate, comprising:

a substrate;

an oxide layer formed over said substrate; and

a plurality of cylindrical contact holes formed in said oxide layer, said plurality of contact holes extending to a topmost surface of said oxide layer and having reduced sidewall striations, thereby reducing critical dimension loss between said contact holes, said reduced sidewall striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma.

60. (Original) The integrated circuit substrate according to claim 59, wherein said substrate is a silicon-based substrate.

61. (Cancelled)

62. (Original) The integrated circuit substrate according to claim 59, wherein said substrate is a germanium substrate.

63. (Cancelled)

64. (Original) The integrated circuit substrate according to claim 59, wherein said substrate is a gallium arsenide substrate.

65. (Cancelled)

66. (Previously presented) The integrated circuit substrate according to claim 59, wherein said substrate further has an antireflective coating thereon.

67. (Original) The integrated circuit substrate according to claim 59, wherein said substrate is a DRAM substrate.

68. (Original) The integrated circuit substrate according to claim 59, wherein said low power plasma is from about 100 Watts to about 250 Watts.

69. (Original) The integrated circuit substrate according to claim 59, wherein said low power plasma is about 150 Watts.

70. (Original) The integrated circuit substrate according to claim 59, wherein said first predetermined time is from about 3 seconds to about 10 seconds.

71. (Original) The integrated circuit substrate according to claim 59, wherein said first predetermined time is about 5 seconds.

72. (Original) The integrated circuit substrate according to claim 59, wherein said high power plasma is from about 800 Watts to about 1100 Watts.

73. (Original) The integrated circuit substrate according to claim 59, wherein said high power plasma is about 950 Watts.

74. (Original) The integrated circuit substrate according to claim 59, wherein said second predetermined time is from about 40 seconds to about 90 seconds.

75. (Original) The integrated circuit substrate according to claim 59, wherein said second predetermined time is about 60 seconds.

76. (Original) The integrated circuit substrate according to claim 59, wherein said low power and said high power plasmas of said etching gas are selected from the group consisting of Cl_2, HBr, CF_4, CHF_3, CH_2F_2, and inert gases.

77. (Original) The integrated circuit substrate according to claim 76, wherein said low power plasma is CH_4, CHF_3 and an inert gas.

78. (Original) The integrated circuit substrate according to claim 76, wherein said high power plasma is CF_4, CHF_3 and an inert gas.

79. (Original) The integrated circuit substrate according to claim 76, wherein said low power plasma includes HBr.

80. (Original) The integrated circuit substrate according to claim 76, wherein said high power plasma includes HBr.

81. (Original) The integrated circuit substrate according to claim 76, wherein said low power plasma includes Cl_2.

82. (Original) The integrated circuit substrate according to claim 76, wherein said high power plasma includes Cl_2.

83. (Original) The integrated circuit substrate according to claim 76, wherein said low power and said high power plasmas are CF_4, CHF_3 and Ar.

84. (Original) The integrated circuit substrate according to claim 76, wherein said low power and said high power plasmas are CF_4, CHF_3 and He.

Claims 85-91. (Cancelled)

92. (Previously presented) An integrated circuit substrate, comprising:

a substrate;

an oxide layer formed over said substrate; and

a plurality of recesses formed in said oxide layer, sidewalls of said recesses forming sidewalls of cylindrical contact holes extending to a topmost surface of said oxide layer and having reduced striations resulting from the application of a first power level plasma of an etching gas to said integrated circuit substrate for a first predetermined time

followed by the application of a second power level plasma of said etching gas to said integrated circuit substrate for a second predetermined time, wherein said second power level plasma is a higher power plasma than said first power level plasma, and wherein said substrate has a decreased critical dimension (CD) loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma.

93. (Previously Presented) The integrated circuit substrate of claim 92, wherein said CD loss is decreased by about 400 Angstroms.

94. (Previously Presented) The integrated circuit substrate of claim 59 wherein the critical dimension loss is reduced by about 400 Angstroms.

95. (Cancelled)